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10EC56

Fifth Semester B.E. Degree Examination, June/July 2018
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Briefly explain the speed / power performance of different technologies. **(04 Marks)**

b. Explain the different steps required for nMOS fabrication process. **(10 Marks)**

c. What is noise margin? Explain CMOS inverter noise margins. **(06 Marks)**

2 a. Explain λ based design rules applicable to wires and contacts. **(10 Marks)**

b. Write the stick diagram and layout for the Fig. Q2 (b). **(05 Marks)**

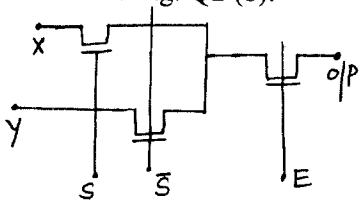

Fig. Q2 (b)

c. Write the layout for two input CMOS NAND gate. **(05 Marks)**

3 Explain the following logic structures with their salient features:

(i) Pseudo nMOS logic (ii) Dynamic CMOS logic

(iii) Clocked CMOS logic (iv) CMOS domino logic. **(20 Marks)**

4 a. Define sheet resistance and standard unit of capacitance. **(02 Marks)**

b. Explain propagation delays with respect to pass transistor chain and long polysilicon wires. **(08 Marks)**

c. Explain scaling factors as applicable to MOS device parameters. **(10 Marks)**

PART – B

5 a. Explain the concept of basic inverting dynamic storage cells and non inverting dynamic storage cells. **(05 Marks)**

b. Briefly explain the basic form of two phase clock generator circuit. **(05 Marks)**

c. Explain bus arbitration logic for n-line bus. **(10 Marks)**

6 a. Explain the concept of carry look ahead adder and represent the 4 bit block CLA unit. **(10 Marks)**

b. Discuss Baugh Wooley method used for two's complement multiplication. **(10 Marks)**

7 a. What are the timing considerations in system design? **(06 Marks)**

b. Explain the read and write operation of a three transistor dynamic RAM memory cell. **(06 Marks)**

c. Explain decoder based selection and control of the 4×4 bit register array. **(08 Marks)**

8 a. Explain input / output pads and represent the 4 bit processor pad utilization **(10 Marks)**

b. With the help of example, explain sensitized path based testing a combinational logic. **(10 Marks)**

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.